TOE-FX101

1G/10G LOW LATENCY
TCP/IP OFFLOAD
ENGINE IP-CORE

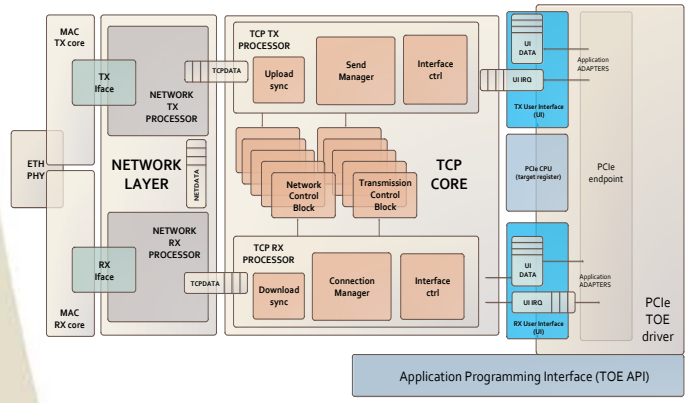
The IP-CORE package is available with TCP echo reference design to evaluate system capabilities and interface communications. A fully optimized PCIe interface can be also available upon request with easy API functions to access the core without any restrictions for your custom software application.

For best performance evaluation the core could be available with its reference hardware board but it is designed to be fully customizable to any FPGA based PCIe board.

The TOE-FX101 could be configured to use only internal FPGA resources (reduced performance). The full performance configuration requires two externals QDRII+ devices.

The TOE-FX 101 test toolkit and simulation model are also available upon request.

TOE-FX101 is an ultra-low latency TCP-IP core engine designed for high-performances network applications. The IP core can interface local area networks at 1G or 10G Ethernet by performing basic Ethernet and Internet Protocol (ARP, ICMP) and RFC based TCP protocol. The TCP header is processed and payload sent to the User Interface with about 100 ns latency. The UI is based on internal BRAM VHDL interface for a quick setup of the IP CORE and easy send/receive operation to develop your full custom hardware application.



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Highlights

- ~100 ns latency
- Open/Close connections
- Port listening
- Send/Receive payload
- Monitor interface
- Configuration interface
- Configurable IP and MAC address
- User Guide
- Reference Design evaluation
- 1G/10G line rate
- TCP window of 32 Kbytes
- 8x available TCP sessions
- MTU of 1536 bytes
- Configurable MSS
- CRC validation
- Nagle's Algorithm
- Out of Order management
- Slow Start
- Congestion avoidance
- Fast Retrasmission/Fast Recovery

RFC compliances

- RFC 791
- RFC 792
- RFC 793
- RFC 826
- RFC 894
- RFC 1122
- RFC 2988
- RFC 5681

Hardware Requirements

- Altera Stratix V
- SFP+ or RJ45 Ethernet connection
- PCIe (optional)
- QDRII+ for full performance

Optionals

- Low latency PCIe with API functions
- Target Board
- Board customization
- Source code
- Test toolkit
- VHDL Simulation models

Ordering Information

1GTFXVHD	1G TOE-FX101 with VHDL user interface
10GTFXVHD	10G TOE-FX101with VHDL user interface
1GTFXPCIe	1G TOE-FX101 with PCIe user interface
10GTFXPCIe	10G TOE-FX101 with PCIe user interface
1GTFXVHD_LW	Lightweight 1G TOE-FX101 with VHDL user interface (only FPGA internal resources)

Please contact us for further details about TOE-FX101 available configurations and options.

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